IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Gilbert Wolrich et al.	Art Unit	: 2143
Serial No.	: 09/473,571	Examiner	: David E. England
Filed	: December 28, 1999	Conf. No.	: 1159
Title	: PROVIDING REAL-TIME CONTROL DATA FOR A NETWORK PROCESSOR		

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REPLY BRIEF

Pursuant to 37 C.F.R. § 41.41, Applicant responds to the Examiner's Answer as follows:

Claims 1-8, 9-17 and 28-32

Responding to appellant's argument that there would is no motivation to combine Isfeld (U.S. 5,592,622) with Chilton (U.S. 6,418,488) and Witkowski (U.S. 6,430,626), the Examiner argued that: "...in the independent claims, it is claimed that 'a push engine to perform unsolicited transfers of the status data to the processing engines in response to the module collecting new status data', or similarly written processing engine, which is not taught by the Appellant's specification nor is the invention enabled to do such." [1]

Appellant contends that this line of reasoning, and the Examiner's conclusion,[2] are improper. The Examiner has neither entered a new rejection in the Examiner's Answer nor has the Examiner ever rejected claim1 or any other claim under 35 U.S.C. 112, first paragraph. Indeed, the newly added 112 rejections referred to by the examiner are directed to §112, second paragraph and are only directed to certain dependent claims.[3] Appellant contends that the examiner never furnished Appellant with notice and the opportunity to respond to any

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[1] Examiner's Answer, page 29.
[2] "Therefore, in view of the above newly added 112 rejection and interpretation as to what Appellant truly teaches in the specification, Isfeld, in view of Chilton and Witkowski teach the push engine's transfer of status information." (Examiner's Answer, page 31).
[3] "Therefore, in view of the above newly added 112 rejection and interpretation as to what Appellant truly teaches in the specification, Isfeld, in view of Chilton and Witkowski teach the push engine's transfer of status information. (Examiner's Answer page 30).
The only 112 rejections made by the examiner were directed to §112, second paragraph rejection over the word "device" and specifically to claims 3, 6 - 8, 10, 14, 21 - 23 and 3, not claim 1

enablement or written description rejections.[4] Therefore, there is no enablement issue before the Board and the Examiner was in error as arguing that claim 1 was not enabled and then based on that argument misconstruing Appellant's claim 1. Therefore, the examiner must take claim 1 as enabled and address the arguments raised by Appellant based on claim 1 and not the examiner's misconstruction of claim 1.

Nevertheless, in order to avoid delays Appellant will address the Examiner's enablement argument. Appellant contends that the specification clearly supports claim 1, as presented and argued by Appellant and that the examiner's interpretation of claim 1 is erroneous and without merit. The specification describes:

> Referring again to FIG. 2, the connections between the FBI 38 and the processing engines 22a-22f are shown. The FBI 38 includes a control module 50 for the ready bus 42 and a push engine 62. The control module 50 periodically collects receive-ready status data and transmit-ready status data from the MAC devices 14, 14', 14". The collected ready status data is stored in a set of status registers 54. The set includes separate registers for storing receive-ready status data and transmit-ready status data. The push engine 62 regularly sends the ready status data over the S bus 39 to scheduler threads located in the processing engines 22a-22f in response to commands from logic internal to the FBI 38.[5]

Thus, Appellant's push engine 62 is part of the FIFO Bus Interface 38. As explained, the push engine 62 sends status data to the processing engines in response to commands from the internal logic of FBI 38 (of which the push engine is part of), but <u>not</u> in response to any command, request or signal from the processing engines 22a-f (e.g., the recipients of the status data). Indeed, the Examiner acknowledges that "[a]ll other areas of the specification state that the FBI 38, as a whole and its individual parts, appears to transfer information unsolicited"[6]

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[4] See MPEP 1207.03, which states "[a]t the time of preparing the answer to an appeal brief, the examiner may decide that he or she should apply a new ground of rejection against some or all of the appealed claims. In such an instance where a new ground of rejection is necessary, the examiner should either reopen prosecution or set forth the new ground of rejection in the answer."

[5] Appellant's specification, page 6, lines 6-18.

[6] Examiner's Answer, Page 30.

Contrary to the examiner's reasoning, the push engine does not randomly send data to some destination, but rather operates in response to some triggering event. However, that triggering event, as noted above, is a command(s) from the FBI 38. Therefore, while the push engine is subordinated to the control mechanism of the module it forms part of, the target recipients (namely, the processing engines) of the status data sent by the push engine do not themselves solicit or request such status data from the push engine.

Accordingly, Appellant's push engine does in fact "perform unsolicited transfers of the status data to the processing engines in response to the module collecting new status data," as required by Appellant's independent claim 1.

The Examiner then incorrectly and improperly mischaracterizes Appellant's claimed invention[7] as corresponding to a "storage memory and/or processor, that sends status information to another processor," relying on col. 27, lines 44 et seq., of Isfeld[8] and the Examiner's interpretation that: "It is clear that the moving of status information from CSB to the RLB and HLB from a command "flush", which could be substantially similar to the a transfer command that is received at the push engine."[9]

In the excerpt from Isfeld[10] relied on by the Examiner, Isfeld fails to describe or suggest the transfer of status data to processing engines such as processing engines recited in Appellant's

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[7] Examiner's Answer, page 31.
[8] Id.
[9] Id.
[10] **H. Message Receive Logic Block**
FIG. 39 shows the structure of the Message Receive Logic Block 410 of FIG. 34. Any data transfer bound for SDRAM moves through this logic. Message and non-message transfers are treated differently: cells which are part of a message transfer are moved into the SDRAM receive buffer structure, while non-message cells do not move into receive buffers--they are written to a specific physical SDRAM address. Quite a bit of the logic in this section is associated with management of the receive buffers and bus logical receive channels.
The major functional blocks are summarized as follows:
Get_free_buffs 500
Maintain status of the double-buffered free list buffer FLB. Post ibus read requests and manage movement of data into the FLB from IBUS. Contains free_head_reg, free_tail_reg, free_start_reg, and free_size_reg registers.
Buffer_alloc 501
Allocate buffers from the FLB to logical receive channels. Read the next sequential FLB entry and write it into the CSB along with a zero count field. Maintain the Channel Status validity register. This module is necessarily quite intimate with an

independent claim 1. Furthermore, Isfeld does not disclose or suggest an unsolicited transfer of status data as recited in Appellant's independent claim 1, using a reasonable[11] interpretation of Appellant's claim 1.

Furthermore, as Appellant explained in its Appeal Brief, Isfeld describes multiple Input/Output Processor (IOP) transferring regular packets (i.e., payload). Isfeld does not describe a transfer, let alone describe an unsolicited transfer of status data. Indeed, by the Examiner's own admission "Isfeld does not specifically teach a module configured to collect status data from devices connected to a bus ..." (Examiner's Answer, page 7), and therefore Isfeld does not disclose transferring such data.

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icb_flush module which needs to mark CSB entries invalid as they are flushed to receive buffers and which needs to check for a valid channel status entry before flushing an ICB message cell to SDRAM.
Rcv_buff_flush 502
Manages the queuing and flushing of completed receive buffers onto the two receive lists maintained in SDRAM. Buffers and status are moved into the rcv and hrcv list buffers (RLB and HLB) by the flush to ibus function. Then, the rcv_buff_flush function manages posting requests to the ibus and the associated flushing of the RLB and HLB.
Msg_rcv_and_icb_fill 503
Moves data from bus into the ICBs. Writes the ICB tags. Performs receive filtering (perhaps).
Flush_to_ibus 504
Reads ICB tags and performs ICB flush to IBUS. "(Isfeld, col. 27, line 31 to col. 28, line 5)

[11] In construing features of claim 1, the Examiner must give the claim elements their broadest reasonable interpretation. The examiner however must be guided by principles set out by the Federal Circuit in cases such as *In re Morris* 127 F.3d 1048, 44 U.S.P.Q.2d 1023, 1027 (Fed. Cir. 1997), which stands for the proposition that while the Office is entitled to construe claim terms using their "broadest reasonable meaning," the Examiner must apply the Court's guidance on what "reasonable" means:

> "Since it would be unreasonable for the PTO to ignore any interpretive guidance afforded by the applicant's written description, either phrasing connotes the same notion: as an initial matter, the PTO applies to the verbiage of the proposed claims the broadest reasonable meaning of the words in their ordinary usage as they would be understood by one of ordinary skill in the art, taking into account whatever enlightenment by way of definitions or otherwise that may be afforded by the written description contained in the applicant's specification." [emphasis supplied]

According to Morris, the examiner must apply the broadest reasonable meaning "in their ordinary usage as they would be understood by one of ordinary skill in the art."

Not only has the examiner failed to provide any 112, first paragraph rejections, the examiner has not provided any basis upon which one skilled in the art would construe in the manner argued by the Examiner.

The Examiner used Chilton to teach: "a module configured to collect status data from devices connected to a bus, the status data indicating readiness of the devices to participate in data transfers, (e.g. col. 25, lines 18 - 59)."[12]

Chilton describes:

> **When the current frame is being transmitted, the hardware checks if a new frame is ready for transmission by checking a next frame ready bit (NxtFrmnRdy) in the transmit status register XmtStat. If the bit is set, the new frame transmission will begin immediately after the current frame is completed, except if a sequence transmission has also been activated, in which case, the sequence transmission takes priority. (Chilton, col. 25, lines 34-40)**

Thus, the current frame will be transmitted if the NxtFrmmRdy is set. Nowhere does Chilton describe that any transfer of the above status information takes place, particularly not to processing engines. Rather, Chilton's status data, stored in the transmit status register, is non-transferable status data. Chilton, therefore, whether taken separately or in combination with Isfeld also fails to disclose or suggest: "unsolicited transfers of status data," as required by Appellant's independent claim 1.

Witkowski, as explained in the Appeal Brief, also fails to disclose or suggest transfer of status data to processing engines. Witkowski merely describes that certain signals are asserted when packets are received in one of the buffers used by Witkowski's system.

Therefore, when the references are viewed as a whole, no combination of these references suggests the claimed features of Appellant's claim 1.

Additionally, Appellant contends that a person of ordinary skill in the art would have no motivation to combine Isfeld's teaching of transfer of packets with the Chilton's teaching of non-transferable status data to "perform unsolicited transfers of status data to the processing engines," as recited in claim 1, nor would the person of ordinary skill combine any of these references with Witkowski's teaching of the non-transferable asserted signals.

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[12] Examiner's Answer, pages 7-8.

In view of the foregoing, Appellant contends that the Examiner failed to establish a *prima facie* case of obviousness for rejecting Appellant's independent claim 1, 9 and 28, and the claims that depend from them.

Claims 33-40

Responding to Appellant's arguments that the Examiner has not identified any aspect of the references teaching the limitations recited in those claims, the Examiner states that:

> **As to the second argument. Appellant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. Furthermore, it is not specifically stated in the Appellant's specification what "multiple multi-threaded engines" could be and is therefore open to what is accepted as a standard definition of a multi-threaded engine could be. It is well known in the art that a multi-threaded engine is nothing more than processors and as very apparent, as described above, the prior art teaches a processing engine. Furthermore, the above interpretation and the specification teachings, in the first response to the remarks, further prove the inconsistency and broadness of the claim language. (Examiner's Answer, pages 31-32)**

Appellant strongly disagrees with the Examiner's contention that Appellant allegedly failed to comply with 37 CFR 1.111(b). As Appellant noted, for example, in the October 13, 2005 Response to Final Office Action:

> "The Examiner also rejected claim 33 with the same argument as claim 1. However, **the Examiner did not even attempt to address a number of limitations of claim 33**. For example, the Examiner has not identified a single feature in any of the cited references as providing "multiple multi-threaded programmable processing engines" as recited in claim 33. As such, the Examiner is requested to withdraw the rejection of claim 33 and its dependent claims." (emphasis in the original, Response to Final Office Action Mailed 07/13/2005, page 11)

Appellant's arguments were in conformance with 37 CFR 1.111(b). 37 C.F.R. §1.104 provides:

37 CFR 1.104 Nature of examination.

(b) *Completeness of examiner's action.* The examiner's action will be complete as to all matters, except that in appropriate circumstances, such as misjoinder of invention, fundamental defects in the application, and the like, the action of the examiner may be limited to such matters before further action is made. However, matters of form need not be raised by the examiner until a claim is found allowable.

As Appellant noted in its Appeal Brief, the Examiner has never provided any reasons for rejecting claims 33-40 which were added in a reply to an outstanding Office Action. When presenting added new claims for examination, an applicant cannot determine *a priori* if such newly added claims may be rejected by an examiner under formal and/or prior art grounds. Rather, upon the presentation of new claims, it is incumbent upon the Examiner to provide a complete examination pursuant to 37 C.F.R. §1.104 and was thus incumbent on the examiner to consider those newly added claims and take action that the Examiner considered appropriate.

With respect to the Examiner's contention that it is not specifically stated in the specification what "multiple multi-threaded engines" are; Appellant contends that the Examiner must apply the plain meaning to the words in the claims.[13] The plain meaning of "multiple multi-threaded engines" is 'more than one multi-threaded processor.' The Examiner's concerns about not being able to determine what "multiple multi-threaded engines" are, therefore, in error.

Appellant further contends that, in any event, independent claim 33, which recites "collect status data of at least one media access device via a bus, the status data indicating whether the at least one media access device has received packet data; and perform a transfer, unsolicited by the programmable processing engines, of at least a portion of the collected status data stored in the at least one register of the interface to at least one register of the multiple multi-threaded programmable processing engines," is patentable over the cited art for reasons similar to those provided herein and in the Appeal Brief with respect to independent claims 1, 9 and 28. Claims 34-40, which depend from independent claim 33, are patentable for at least the same reasons as independent claim 33.

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[13] See 2111.01 Plain Meaning [R-5]

Claims 18-27

Responding to Appellant's arguments that no motivation exists for combining Ebrahim (U.S. 5,887,134) with Gulledge (U.S. 5,644,623) and Witkowski, the Examiner stated:

> **The motivation for the combination of Ebrahim and Gulledge can be further understood as when information is gathered and transmitted automatically in response to a condition it would be a faster transmission of information because one does not have to request information from a device or memory in order to receive said information. It would be understood that when information is sent using a trigger type response it would cut out any need for a request. It is also noted that utilizing information about measurements as found in Gulledge could be used to find a state or status of a device or portion of a device and its work load or capability, example, enough memory to store information or if transmission or buffer lines are full and nothing can be transferred. (Examiner's Answer, pages 32-33)**

Ebrahim is directed to computer nodes with interfaces that transmit data. In contrast, and as explained in Appellant's Appeal Brief, Gulledge describes a system that automatically collects historic statistics about the quality of service experiences by different handsets of a cellular phone network. Therefore, in view of the disparate technologies that the Examiner proposes to combine, Appellant contends that a person of ordinary skill in the art would not have the motivation to combine Gulledge's teaching of sporadic collection of statistics of quality of service of cellular telephone handsets with Ebrahim's teaching of fast rate network data transmissions.

Accordingly, Appellant submits that the Examiner has failed to establish a *prima facie* case of obviousness for rejecting independent claim 18 and its dependent claims.

Claims 3, 6-8, 10, 14, 21-23 and 31

Responding to Appellant's arguments that an antecedent basis exists for the term "the devices", the Examiner stated:

> **As to the fourth argument, the Appellant's claims state media access devices. It is unclear if the Appellant is attempting to bring in another, separate and distinct, "device" as stated in claims mentioned above. Therefore it can be interpreted that there are two "sets" of devices, one being "media access devices" and the other being just "devices". In the Appellant's amendment after final it was clear that it was only mean to teach "media access devices" but now there is only one set of devices that are present, not two as could previously be interpreted. (Examiner's Answer, page 34)**

In its reply to the Final Action, Appellant sought to clarify any alleged indefiniteness by adding the wording "media access" before the word "devices" in the above-mentioned claims. The Examiner, however, did not enter those amendments.[14]

Nevertheless, Appellant contends that it is clear from the language of the above-identified claims that "devices" refers to the "media access devices" recited in the claims from which the above claims depend. A claim is indefinite when it contains words or phrases whose meaning is unclear.[15] There exists but one recitation of "devices" in each of independent claims 1, 9 and 28, namely "media access devices." Thus, the subsequent recitation of "devices" in claims depending from those independent claims clearly refers to the "media access devices" recited in claim 1. Appellant contends that the meaning of "devices" appearing in the rejected claims is reasonably ascertainable by one skilled in the art as a short-hand expression for the more cumbersome "media access devices."

It is well settled that the failure to provide explicit antecedent basis for terms does not always render a claim indefinite. If the scope of a claim would be reasonably ascertainable by those skilled in the art, then the claim is not indefinite. *Energizer Holdings Inc. v. Int'l Trade Comm'n*, 435 F.3d 1366, 77 USPQ2d 1625 (Fed. Cir. 2006) (holding that "anode gel" provided by implication the antecedent basis for "zinc anode"); *Ex parte Porter*, 25 USPQ2d 1144, 1145 (Bd. Pat. App. & Inter. 1992) ("controlled stream of fluid" provided reasonable antecedent basis for "the controlled fluid").

Therefore, contrary to the Examiner's contentions, claims 3, 6-8, 10, 14, 21-23 and 31 are not rendered indefinite for not fully reciting "media access" in front of "devices."

Claim 39

Responding to the Appellant's argument that the recitation "the at least one media access device comprises multiple media access devices" is not contradictory with the claim 33 recitation "at least one media access device," the Examiner stated:

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[14] Although entry of Amendments after final are at the discretion of the examiner, clearly those directed to removing minor informalities and simplifying issues on appeal as that one sought to do should be enterable by the examiner exercising reasonable discretion.
[15] See MPEP 2173.05(e).

> **As to the fifth argument, it still seem that the way the Appellant has worded the claim appears to be contradictory in the one interpretation, "How can one be multiple?" It is agreed that at least one could be more than one but it still can be one. If the Appellant amended to state at least 2, it would not contradict the one interpretation because now there would have to be two which falls under multiple. (Examiner's Answer, page 35)**

Appellant submits that the recitation of claim 39 is directed to those embodiments that do not have just a single media access device. Specifically, claim 39 is directed to embodiments that have more than one media access device.

Accordingly, the Examiner's contention that the claim language could include one media access device is unfounded and inapplicable to the embodiments sought to be protected by the claim language of claim 39.

Claim 40

Responding the Appellant's arguments regarding the language "the status data of multiple media access devices is stored in a single one of the at least one register of the interface," the Examiner stated:

> As to the final argument, Examiner means the status data of multiple media access devices would mean that there are different status data and that "at least one register of the interface" would mean that all the different status data could be stored in one register, or each multiple media access device would have their own register to store status data in, etc. Furthermore, it is unclear as to what is mean by "a single one of the at least one register". Would that mean it is only one register or there is only a single status data stored in one register, multiple registers, etc. Appellant still has not clarified what is meant by the above limitation nor has given examples or sections of the specification to support this limitation and clarify its meaning. (Examiner's Answer, page 36)

The plain and ordinary meaning of the language recited in claim 40 is that; in those embodiments to which claim 40 is directed, the status data of media access devices is stored in a single register. In contrast, for example, in some of embodiments of claim 33, from which claim 40 depends, the status data of media access devices may be stored in multiple registers, as provided by the language "at least one register." Appellant's notes that the language "at least one register" includes one register or multiple register, and that claim 40 merely seeks to delineate the situations in which only one register is used to store status data of media access devices. Accordingly, Appellant submits that the recitation "the status data of multiple media

access devices is stored in a single one of the at least one register of the interface" is amply clear and not indefinite.

Conclusion

For the foregoing reasons, and the reasons stated in the Appeal Brief, appellant submits that the final rejection should be reversed.

Please apply any required fees or credits to deposit account 06-1050, referencing the attorney docket number shown above.

Respectfully submitted,

Date: 3/16/07

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